S.B. Roll No……

VLSI SYSTEM DESIGN
6th Exam/ECE/3613/Jun'2021
(For 2018 Batch onwards)

Duration: 1.15Hrs. **M.Marks:25**

SECTION-A

Q1. Attempt any three questions. **3x5=15**

i. What are the advantages of VHDL?
ii. What is the difference between an entity and architecture declaration?
iii. Write a short note on Test benches.
iv. Explain the structural style in VHDL architecture.
v. Write VHDL code for four bit register with asynchronous clear.
vi. Write down the features of GAL.
vii. Differentiate between CASE statement and IF-ELSE statement.

SECTION-B

Q2. Attempt any one question. **1x10=10**

a. Write a VHDL code for 8:1 MUX using CASE statement.
b. Wirte a VHDL code for 8:3 binary encoder using IF statement.
c. Differentiate between signal statement and variable statement.
d. Draw the schematic diagram of 4 bit full addar and write down its structural modeling.