S.B. Roll No……

VLSI SYSTEM DESIGN
6th Exam/ECE/3613/Jan'2022
(FOR 2018 BATCH ONWARDS)

Duration: 1.15Hrs. **M.Marks:25**

SECTION-A

Q1. Attempt any three questions. **3x5=15**

i. Explain the internal architecture of FPGA.
ii. Design a 3 to 8 bit decoder and write vhdl code for it?
iii. What is VLSI Design?
iv. What are the different modelling styles used in VHDL?
v. Write down the VHDL code for 4:1 multiplexer?
vi. What can be the various uses of VHDL?
vii. Compare CPLD and FPGA?

SECTION-B

Q2. Attempt any one question. **1x10=10**

a. Explain different operators used in VHDL?
b. Explain the composite and scalar data types
c. Write short note on (A) ROM (B)CPLDs
d. Differentiate combinational and Sequential circuits?