S.B. Roll. No……

DIGITAL ELECTRONICS
3rd Exam/ECE/IT/CSE/0195/Jun'2022
(For 2018 Batch Onwards)

Duration: 3Hrs. **M.Marks:75**

SECTION-A

Q1. Do as directed. **15x1=15**

a. The no. of bits in a nibble is _____.
b. Octal system uses digits from_____.
c. Decimal 8 in excess-3 code is _____.
d. A+ (B.C) = _____.
e. BCD stands for_____.
f. _____ changes serial data into parallel data.
g. A Half adder adds _____ bits.
h. _____ And _____ are UNIVERSAL gates.
i. A flip flop is memory element.(T/F)
j. EPROM is available in all technologies.(T/F)
k. ASCII stands for_____.
l. 4:1 Multiplexer has _____ number of select lines.
m. Race around condition can be avoided by using Master Slave JK flip flop .(T/F)
n. PIPO stands for _____.
o. LED stands for_____.

SECTION-B

Q2. Attempt any six questions. **6x5=30**

i. Differentiate between Analog and Digital signals?
ii. Draw and explain the circuit for half subtractor?
iii. Define SSI, MSI, LSI, VLSI and ULSI?
iv. What is a T flip flop? Show its symbol and draw truth table for negative edge triggered T flip flop?
v. Draw logic circuit of 4:1 multiplexer and explain its working?
vi. Differentiate between asynchronous and synchronous counters?
vii. Explain the working of decade counter?
viii. Draw the circuit of parallel in- parallel out shift register and explain its working?

SECTION-C

Q3. Attempt any three questions. **3x10=30**

a. Explain working and construction of JK flip flop. How Race around condition can be avoided by using Master Slave JK flip flop?
b. Define logic gate? Explain various logic gates along with symbols and truth tables?
c. Minimize and implement in SOP form
   $F(A, B, C, D) = \sum m(1, 2, 3, 6, 8, 12, 14, 15)$
d. Draw and explain the circuit for half adder and full adder?
e. Explain the following i) Universal shift registers ii) seven segment display