S. B. Roll. No……

**VLSI SYSTEM DESIGN**
**6th Exam/ECE/3613/Jun'2022**
**(For 2018 Batch Onwards)**

**Duration: 3Hrs.** **M.Marks:75**

**SECTION-A**

**Q1. Give answer in one line.** **15x1=15**

a. Will the entity name 'xyz' and 'XYZ' be treated the same in VHDL?
b. Among the VHDL features, which language statements are executed at the same time in parallel flow?
c. List out the various modes for Port in VHDL.
d. List out the levels of abstractions in VHDL.
e. Which type of Assignment statements will be used in Behavioural level?
f. Which is the Signal assignment operator?
g. Write the full form of VHDL.
h. Can a counter be implemented with concurrent statements only?
i. How many styles of loop statement does the VHDL have?
j. What does a PLA contain?
k. What does FPGA stand for?
l. What kind of statement is the IF statement?
m. On which side of assignment operator, we can use the IN type signal?
n. Which is the default mode for a port variable?
o. In which part of the VHDL code, generics are declared?

**SECTION-B**

**Q2. Attempt any six questions.** **6x5=30**

i. What is VHDL? State its various features.
ii. State and explain the entity in VHDL.
iii. State the differences between Concurrent and Sequential statements.
iv. Explain the importance of clock in sequential circuits. How clock is implemented in VHDL?
v. Explain the process statement with example.
vi. Compare CPLD and FPGA.
vii. How PLA is different from PAL?
viii. Write a VHDL program to build a 4-bit binary counter.

**SECTION-C**

**Q3. Attempt any three questions.** **3x10=30**

a. What are the different types of VHDL modelling? Explain them with example.
b. Write VHDL Code for 4:1 Mux using i) if statement ii) case statement
c. Explain the basic architecture of PLA. State its advantages, disadvantages and applications.
d. Write the VHDL code for the following logical expression:
   $Y=\sum m\ (1, 2, 9, 10, 11, 14, 15)$
e. With the help of block diagram explain ASIC Design flow.