S. B. Roll. No.....

VLSI SYSTEM DESIGN
6th Exam/ECE/3613/Dec'22
(For 2018 Batch Onwards)

Duration: 3Hrs. **M.Marks:75**

SECTION-A

Q1. Do as directed. **15x1=15**

a. VHDL stands for_____
b. FPAA stands for_____
c. PEEL stands for_____
d. PLAs stands for_____
e. VHDL models can be of _____, _____ and _____types.
f. Operator which calculates MODULUS in VHDL is _____.
g. Symbol for "not equal to" sign in VHDL is _____.
h. Architecture of an entity defines _____ functionality.
i. A basic identifier in VHDL is composed of a _____of one or more characters.
j. An entity declaration describes _____ of the entity.
k. Concatenation (&) operator is in _____operators.
l. _____ is used at the end of the statement in VHDL language.
m. Access types are similar to _____ in traditional programming languages.
n. Port names consist of lettes, digits and underscore. (T/F)
o. VHDL is an event-driven language. (T/F)

SECTION-B

Q2. Attempt any six questions. **6x5=30**

i. List down various features of VHDL.
ii. Write a VHDL code for half adder using Dataflow style of modelling.
iii. What is the difference between GAL and PAL?
iv. What is a operator overloading? Explain its use in VHDL.
v. Explain Process statement with example.
vi. What is entity declaration? Write its syntax.
vii. Differentiate between concurrent statement and sequential statement.
viii. Write a VHDL code for 2-to-1 multiplexer.

SECTION-C

Q3. Attempt any three questions. **3x10=30**

a. Explain behavioral, dataflow and structural modelling techniques with example.
b. Compare CPLDs and FPGA in detail.
c. Design BCD to Gray code converter using VHDL language.
d. Explain conventional ASIC design flow in detail.
e. Explain different operators used in VHDL language.
f. Design a sequential circuit of 4-bit down counter with VHDL.